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DSP56858EVMUM/D
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DSP56858 Evaluation Module

User's Manual

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Preface

This reference manual describes in detail the hardware on the DSP56858 Evaluation Module.

Audience

This document is intended for application developers who are creating software for devices using the Motorola DSP56858 part.

Organization

This manual is organized into two chapters and two appendixes.

- **Chapter 1, Introduction -** provides an overview of the EVM and its features.
- **Chapter 2, Technical Summary -** describes in detail the DSP56858 hardware.
- **Appendix A, DSP56858EVM Schematics -** contains the schematics of the DSP56858EVM.
- **Appendix B, DSP56858EVM Bill of Material -** provides a list of the materials used on the DSP56858EVM board.

Suggested Reading

More documentation on the DSP56858 and the DSP56858EVM kit may be found at URL:

http://www.mot.com/SPS/DSP/documentation/index.html

Notation Conventions

This manual uses the following notational conventions:

Term or Value	Symbol	Examples	Exceptions
Active High Signals (Logic One)	No special symbol attached to the signal name	A0 CLKO	
Active Low Signals (Logic Zero)	Noted with an overbar in text and in most figures	$\overline{\text{WE}}$ $\overline{\text{OE}}$	In schematic drawings, Active Low Signals may be noted by a backslash: /WE
Hexadecimal Values	Begin with a "$" symbol	$0FF0 $80	
Decimal Values	No special symbol attached to the number	10 34	
Binary Values	Begin with the letter "b" attached to the number	b1010 b0011	
Numbers	Considered positive unless specifically noted as a negative value	5 -10	Voltage is often shown as positive: +3.3V
Blue Text	Linkable on-line	...refer to Chapter 7, License	
Bold	Reference sources, paths, emphasis	...see: **http://www.mot.com/SPS/DSP...**	

Definitions, Acronyms, and Abbreviations

Definitions, acronyms and abbreviations for terms used in this document are defined below for reference..

Codec COder/DECoder; a part used to convert analog signals to digital (coder) and digital signals to analog (decoder)

DIP Dual Inline Package

DSP Digital Signal Processor or Digital Signal Processing

EEPROM Electrically Erasable Programmable Read-Only Memory

EOnCE	Enhanced On-Chip Emulation; a debug bus and port created by Motorola to enable a designer to create a low-cost hardware interface for a professional quality debug environment
ESSI	Enhanced Synchronous Serial Interface; a communications port on Motorola's family of DSPs
EVM	Evaluation Module; a hardware platform which allows a customer to evaluate the silicon and develop his application.
GPIO	General Purpose Input and Output port on Motorola's family of DSPs; does not share pin functionallity with any other peripheral on the chip and can only be set as an input, output or level-sensitive interrupt input
HI	Host Interface; a communications port on Motorola's family of DSPs
IC	Integrated Circuit
JTAG	Joint Test Action Group; a bus protocol/interface used for test and debug
LED	Light Emitting Diode
LQFP	Low Profile Quad Flat Pack package
MPIO	Multi Purpose Input and Output port on Motorola's family of DSPs; shares package pins with other peripherals on the chip and can function as a GPIO
PCB	Printed Circuit Board
PLL	Phase Locked Loop
RAM	Random Access Memory
ROM	Read Only Memory
SCI	Serial Communications Interface; a communications port on Motorola's family of DSPs
SPI	Serial Peripheral Interface; a communications port on Motorola's family of DSPs
SRAM	Static Random Access Memory
SSI	Synchronous Serial Interface; a communications port on Motorola's family of DSPs

THD Total Harmonic Distortion

USB Universal Serial Bus

WS Wait State

References

The following sources were referenced to produce this manual:

[1] DSP56800E Reference Manual, DSP56800ERM/D

[2] DSP5685x 16-Bit Digital Signal Processor User's Manual, DSP5685xUM/AD

[3] DSP56858 16-Bit Digital Signal Processor Technical Data, DSP56858/D

Chapter 1
Introduction

The DSP56858EVM is used to demonstrate the abilities of the DSP56858 and to provide a hardware tool allowing the development of applications that use the DSP56858.

The DSP56858EVM is an evaluation module board that includes a DSP56858 part, 16-bit stereo codec, USB 1.1/2.0 interface, external memory and a daughter card expansion interface. The daughter card expansion connectors are for signal monitoring and user feature expandability.

The DSP56858EVM is designed for the following purposes:

- Allowing new users to become familiar with the features of the 56800E architecture. The tools and examples provided with the DSP56858EVM facilitate evaluation of the feature set and the benefits of the family.
- Serving as a platform for real-time software development. The tool suite enables the user to develop and simulate routines, download the software to on-chip or on-board RAM, run it, and debug it using a debugger via the JTAG/Enhanced OnCE (EOnCE) port. The breakpoint features of the EOnCE port enable the user to easily specify complex break conditions and to execute user-developed software at full speed until the break conditions are satisfied. The ability to examine and modify all user-accessible registers, memory and peripherals through the EOnCE port greatly facilitates the task of the developer.
- Serving as a platform for hardware development. The hardware platform enables the user to connect external hardware peripherals. The on-board peripherals can be disabled, providing the user with the ability to reassign any and all of the DSP's peripherals. The EOnCE port's unobtrusive design means that all memory on the board and on the DSP chip is available to the user.

1.1 DSP56858EVM Architecture

The DSP56858EVM facilitates the evaluation of various features present in the DSP56858 part. The DSP56858EVM can be used to develop real-time software and hardware products based on the DSP56858. The DSP56858EVM provides the features necessary

for a user to write and debug software, demonstrate the functionality of that software and interface with the customer's application-specific device(s). The DSP56858EVM is flexible enough to allow a user to fully exploit the DSP56858's features to optimize the performance of his product, as shown in **Figure 1-1**.

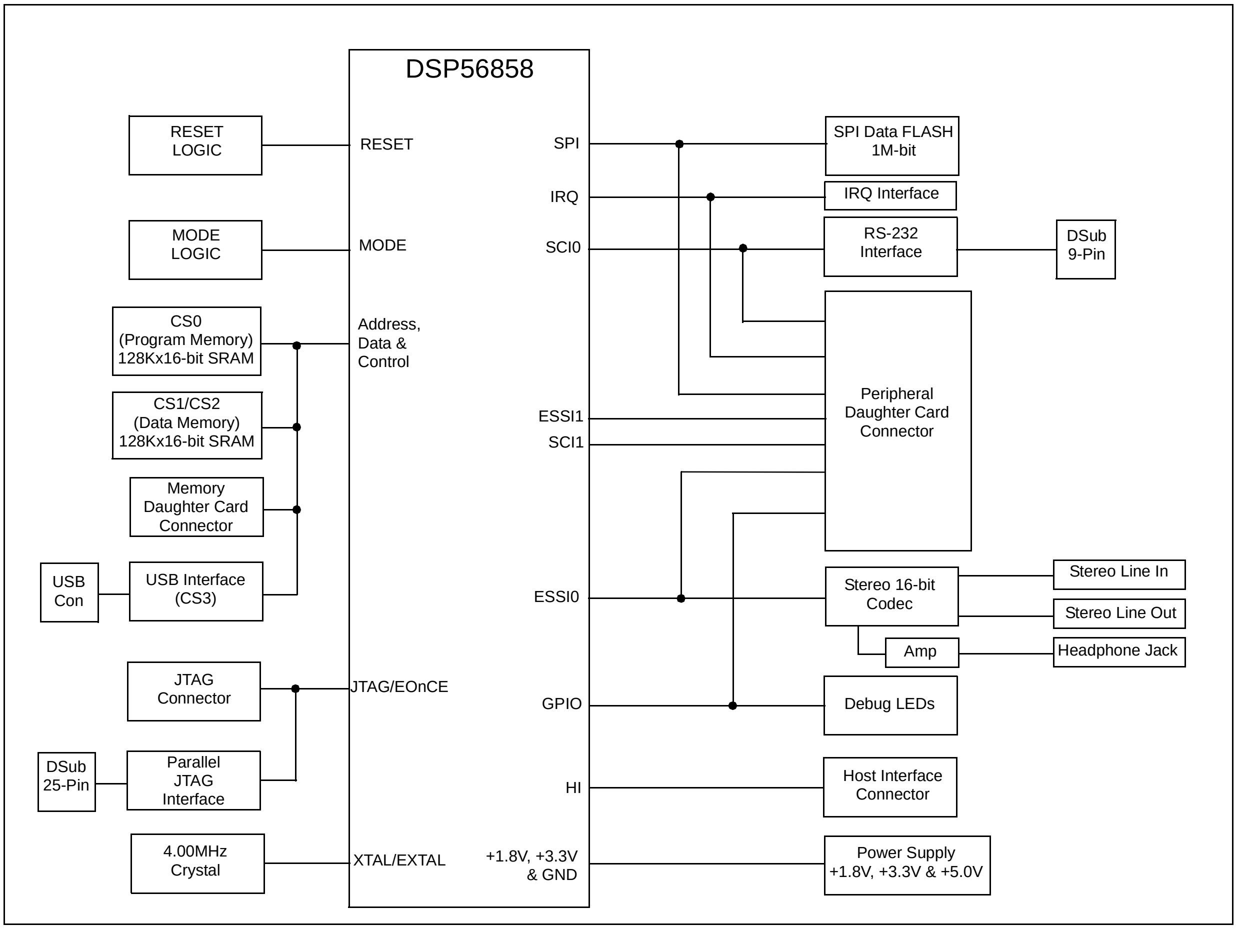


Figure 1-1. Block Diagram of the DSP56858EVM

1.2 DSP56858EVM Configuration Jumpers

Ten jumper groups, (JG1-JG11), shown in **Figure 1-2**, are used to configure various features on the DSP56858EVM board. **Table 1-1** describes the default jumper group settings.

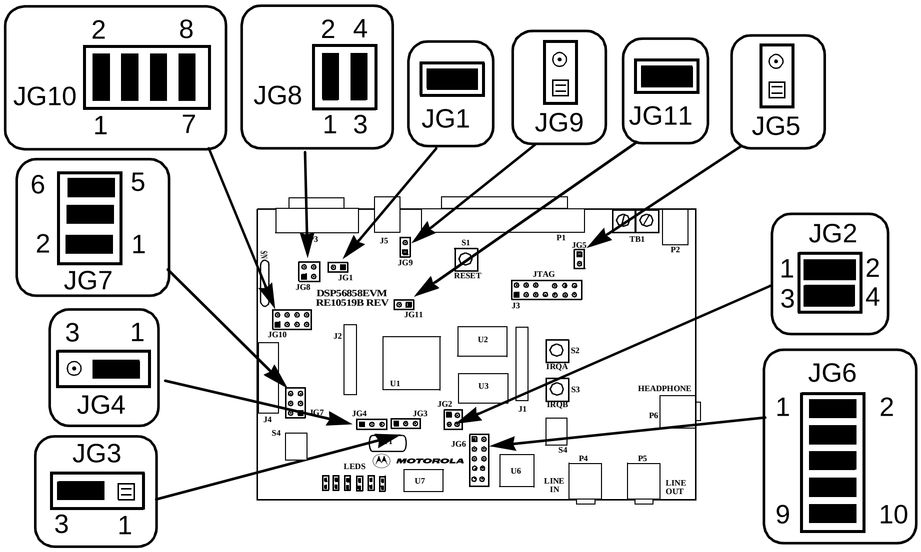


Figure 1-2. DSP56858EVM Jumper Reference

Table 1-1. DSP56858EVM Default Jumper Options

Jumper Group	Comment	Jumpers Connections
JG1	Enable on-board Word selectable SRAM via CS0 (U2)	1–2
JG2	Enable on-board Byte selectable SRAM via CS1/CS2 (U3)	1-2, 3-4
JG3	Use on-board EXTAL crystal input for DSP oscillator	2–3
JG4	Use on-board XTAL crystal input for DSP oscillator	1–2
JG5	Enable on-board Parallel JTAG Host/Target Interface	NC
JG6	Enable ESSI0 Port for CODEC data	1-2, 3-4, 5-6, 7-8, 9-10
JG7	Enable GPIO for CODEC control	1-2, 3-4, 5-6
JG8	Enable SCI0 Port to RS-232 transceiver	1–2, 3-4
JG9	Enable RS-232 output	NC
JG10	Enable SPI Port to Serial EEPROM/Data FLASH	1–2, 3–4, 5–6 & 7–8
JG11	Enable USB interface via CS3	1-2

1.3 DSP56858EVM Connections

An interconnection diagram is shown in **Figure 1-3** for connecting the PC and the external +12.0V DC/AC power supply or external +5.0V DC lab power supply to the DSP56858EVM board.

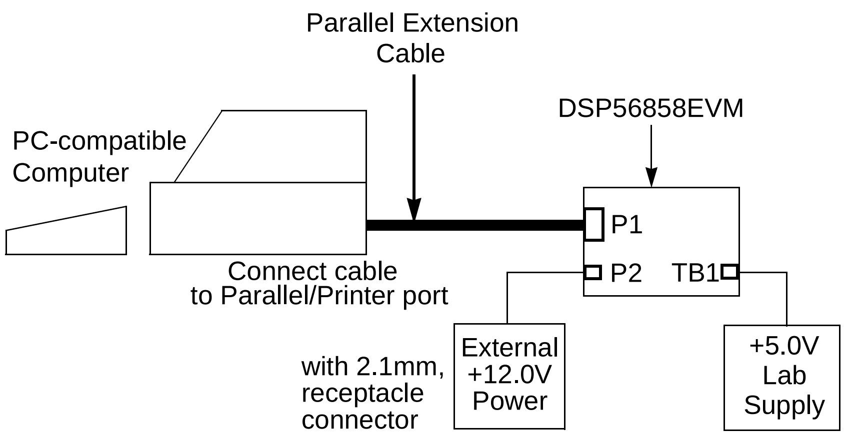


Figure 1-3. Connecting the DSP56858EVM Cables

Perform the following steps to connect the DSP56858EVM cables:

1. Connect the parallel extension cable to the Parallel port of the host computer.
2. Connect the other end of the parallel extension cable to P1, shown in **Figure 1-3**, on the DSP56858EVM board. This provides the connection which allows the host computer to control the board.
3. Make sure that the external +12.0V DC 1.2A switching power supply or the external +5.0V DC 1A lab power supply is not plugged into a +120V AC power source.
4. Connect the 2.1mm output power plug from the external switching power supply into P2, shown in **Figure 1-3**, on the DSP56858EVM board. Optionally, attach an external +5.0V DC lab power supply via the 2-pin terminal block, TB1.
5. Apply power to the external power supply. The green Power-On LED, LED7, will illuminate when power is correctly applied.

Chapter 2
Technical Summary

The DSP56858EVM is designed as a versatile Digital Signal Processor, (DSP), development card for developing real-time software and hardware products to support a new generation of applications in digital and wireless messaging, digital answering machines, feature phones, modems, and digital cameras. The power of the 16-bit DSP56858 DSP, combined with the on-board 128K × 16-bit external program/data static RAM (SRAM), 128K × 16-bit external data/program SRAM, RS-232 interface, Stereo 16-bit codec interface, USB 2.0 interface, Daughter Card Expansion interface and parallel JTAG interface, makes the DSP56858EVM ideal for developing and implementing many audio and voice algorithms, as well as for learning the architecture and instruction set of the DSP56858 processor.

The main features of the DSP56858EVM, with board and schematic reference designators include:

- DSP56858 16-bit +1.8V/+3.3V Digital Signal Processor operating at 120MHz [U1]
- External fast static RAM (FSRAM) memory, configured as:
  - — 128K×16-bit of memory [U2] with one wait state at 120MHz via CS0
  - — 128K×16-bit of memory [U3] with one wait state at 120MHz via CS1/CS2
- 1M-bit Serial EEPROM/Data FLASH [U4]
- 4.00MHz crystal oscillator for DSP frequency generation [Y1]
- Optional external oscillator frequency input connectors [JG3 and JG4]
- Joint Test Action Group (JTAG) port interface connector for an external debug Host Target Interface [J3]
- On-board Parallel JTAG Host Target Interface, with a connector for a PC printer port cable [P1]
- RS-232 interface for easy connection to a host processor [U5 and P3]
- 16-bit stereo codec interface [U6, JG6, JG7, P4 and P5]
- Stereo headphone interface [U8 and P6]
- Codec sample rate selector [S5]

- USB interface [U15and J5]
- Peripheral Daughter Card Expansion Connector, to allow the user to connect his own SCI, ISSI, SPI or GPIO-compatible peripheral to the DSP [J2]
- Memory Daughter Card Expansion Connector, to allow the user to connect his own memory or memory device to the DSP [J1]
- Host Interface Connector, for high-speed bus data transfer [J4]
- On-board power regulation from an external +12V DC-supplied power input [P2]
- On-board power regulation from an optional +5V DC-supplied power input [TB1]
- Light Emitting Diode (LED) power indicator [LED7]
- Six on-board real-time user debugging LEDs [LED1-6]
- Boot MODE selector [S4]
- Manual RESET push-button [S1]
- Manual interrupt push-button for $\overline{\text{IRQA}}$ [S2]
- Manual interrupt push-button for $\overline{\text{IRQB}}$ [S3]

2.1 DSP56858

The DSP56858EVM uses a Motorola DSP56858FV120 part, designated as U1 on the board and in the schematics. This part will operate at a maximum speed of 120MHz. A full description of the DSP56858, including functionality and user information, is provided in these documents:

- *DSP56858 Technical Data*, (DSP56858/D)**:** Provides features list and specifications, including signal descriptions, DC power requirements, AC timing requirements and available packaging
- *DSP5685x User's Manual*, (DSP5685xUM/AD): Provides an overview description of the DSP and detailed information about the on-chip components, including the memory and I/O maps, peripheral functionality, and control/status register descriptions for each subsystem
- *DSP56800E Reference Manual*, (DSP56800ERM/D): Provides a detailed description of the core processor, including internal status and control registers and a detailed description of the family instruction set

Refer to these documents for detailed information about chip functionality and operation. They can be found on this URL:

http://www.motorola.com/semiconductors

2.2 Program and Data Memory

The DSP56858EVM contains two 128Kx16-bit Fast Static RAM banks. SRAM bank 0 is controlled by CS0 and SRAM bank 1 is controlled by CS1 and CS2.

2.2.1 SRAM Bank 0

SRAM bank 0, which is controlled by CS0, uses a 128K×16-bit Fast Static RAM (GSI GS72116, labelled U2) for external memory expansion; see the FSRAM schematic diagram in **Figure 2-1**. CS0 can be configured to use this memory bank as 16-bit program memory, data memory, or both. Additionally, CS0 can be configured to assign this memory's size and starting address to any modulo address space.

This memory bank will operate with one wait state access while the DSP56858 is running at 120MHz and can be disabled by removing the jumper at JG1.

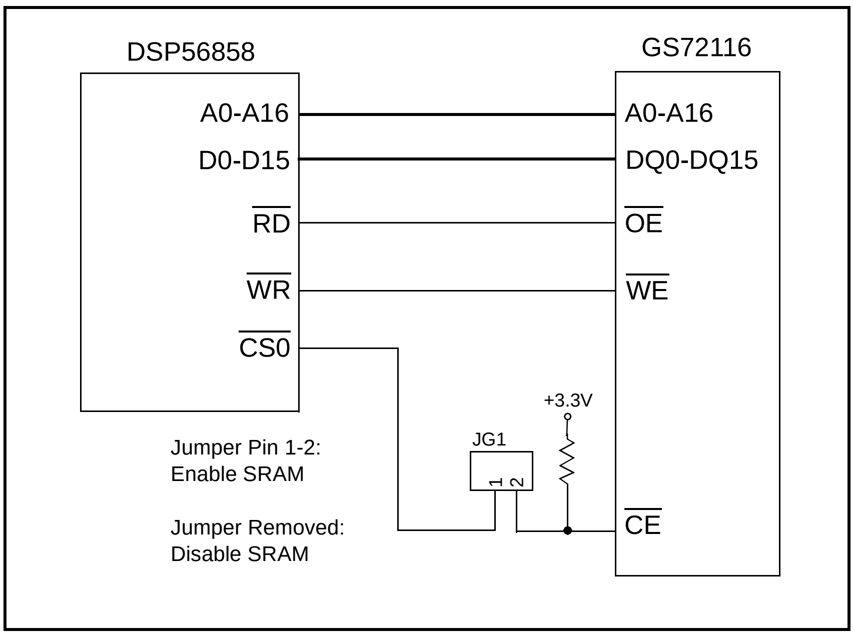


Figure 2-1. Schematic Diagram of the External CS0 Memory Interface

2.2.2 SRAM Bank 1

SRAM bank 1, which is controlled by CS1 and CS2, uses a 128K×16-bit Fast Static RAM (GSI GS72116, labelled U3) for external memory expansion; see the FSRAM schematic diagram in **Figure 2-2**. Using CS1 and CS2, this memory bank can be configured as byte (8-bit) or word (16-bit) accessable program memory, data memory, or both. Additionally,

CS1 and CS2 can be configured to assign this memory's size and starting address to any modulo address space.

This memory bank will operate with one wait state access while the DSP56858 is running at 120MHz and can be disabled by removing the jumpers at JG2.

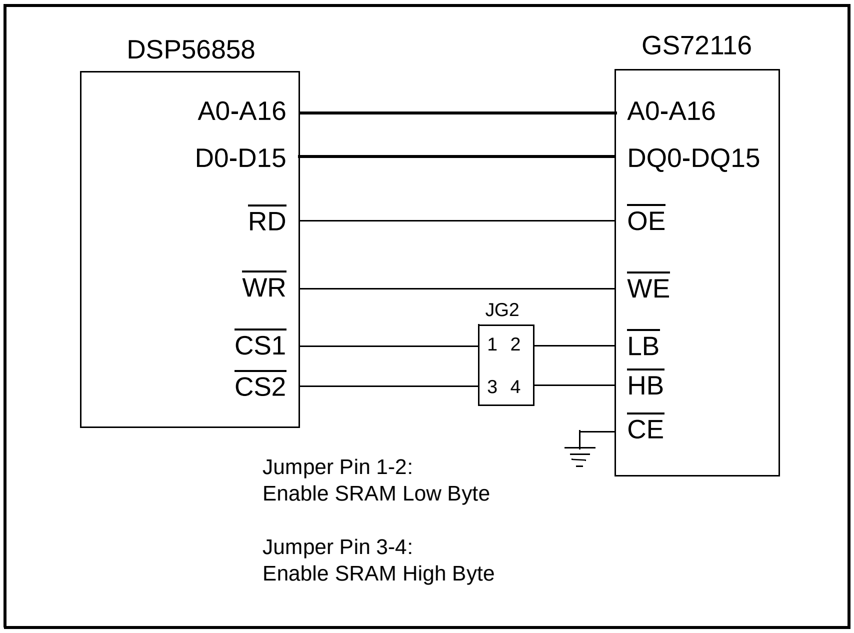


Figure 2-2. Schematic Diagram of the External CS1/CS2 Memory Interface

2.3 SPI Serial EEPROM/Data FLASH Memory

A 1M-bit +3.3V SPI serial EEPROM/Data FLASH Memory, Atmel AT45DB011B-SC, is provided on the DSP56858EVM, reference **Figure 2-3**. This memory connects directly to the SPI Port through a header on the DSP56858. It can be used to load program code and data into the DSP56858's internal or external memory spaces. Jumper block JG10 is provided to allow the user to disconnect the on-board SPI EEPROM/Data FLASH from the SPI port and allow him to connect his own SPI port peripheral. The header details are shown in **Table 2-1**.

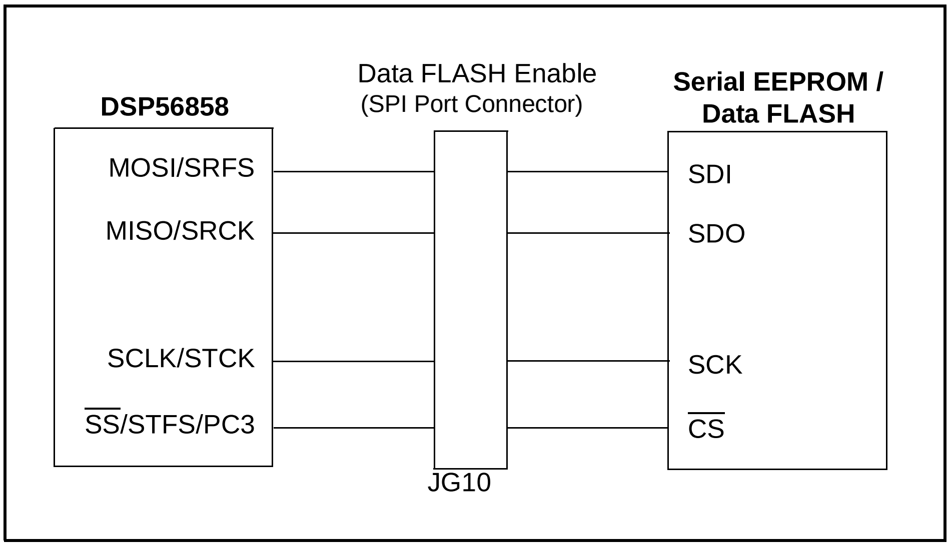


Figure 2-3. SPI EEPROM Memory Block Diagram

Table 2-1. SPI Port Connector Description

JG10			
Pin #	**Signal**	**Pin #**	**Signal**
1	$\overline{SS}$/PF3	2	$\overline{CS}$
3	MISO/PF0	4	SDO
5	MOSI/PF1	6	SDI
7	SCK/PF2	8	SCK

2.4 RS-232 Serial Communications

The DSP56858EVM provides an RS-232 interface by the use of an RS-232 level converter, (Maxim MAX3245EEAI, designated as U5). Refer to the RS-232 schematic diagram in **Figure 2-4**. The RS-232 level converter transitions the SCI UART's +3.3V signal levels to RS-232-compatible signal levels and connects to the host's serial port via connector P3. Flow control is not provided, but could be implemented using uncommitted GPIO signals. The pinout of connector P3 is listed in **Table 2-2**. The RS-232 level converter/transceiver can be disabled by placing a jumper at JG9.

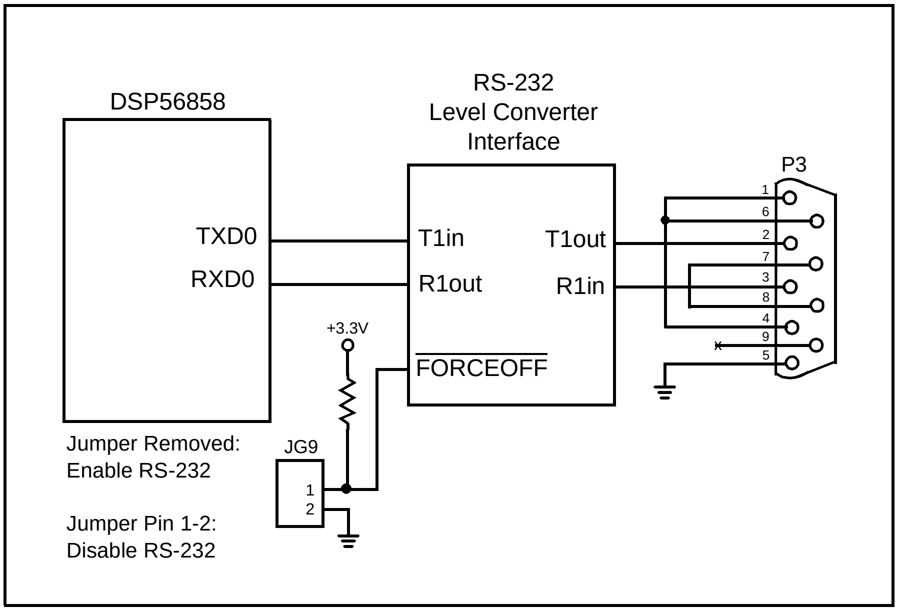


Figure 2-4. Schematic Diagram of the RS-232 Interface

Table 2-2. RS-232 Serial Connector Description

P3			
Pin #	**Signal**	**Pin #**	**Signal**
1	Jumper to 6 & 4	6	Jumper to 1 & 4
2	TXD0	7	Jumper to 8
3	RXD0	8	Jumper to 7
4	Jumper to 1 & 6	9	N/C
5	GND		

2.5 Clock Source

The DSP56858EVM uses a 4.00MHz crystal, Y1, connected to its external crystal inputs, EXTAL and XTAL. To achieve its 120MHz maximum operating frequency, the DSP56858 uses its internal PLL to multiply the input frequency by 30. An external oscillator source can be connected to the DSP by using the oscillator bypass connectors, JG3 and JG4; see **Figure 2-5**. If the input frequency is above 4MHz, then the EXTAL input should be jumpered to ground by adding a jumper between JG4 pins 1 and 2. The input frequency would then be injected on JG3's pin 2. If the DSP needs to be synchronized to the codec's sample frequency, then the DSP's input frequency should be jumpered using the 12.2280MHz codec frequency. If the input frequency is below 4MHz, then the input frequency can be injected on JG4's pin 2.

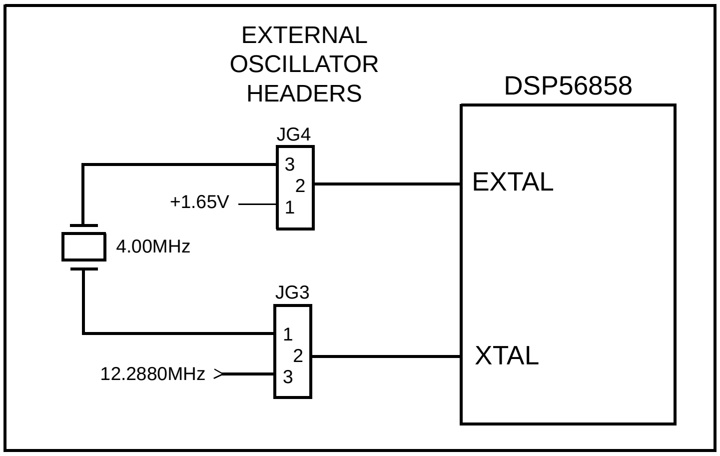


Figure 2-5. Schematic Diagram of the Clock Interface

2.6 Operating Mode

The DSP56858EVM provides a boot-up MODE selection switch, S4. This switch is used to select the operating mode of the DSP as it exits RESET. Refer to the DSP56858 User's Manual for a complete description of the chip's operating modes. **Table 2-3** shows the two operation modes available on the DSP56858.

Table 2-3. Operating Mode Selection

Operating Mode	S4 (ON)	Comment
0	1–2, 3-4 & 5-6	Bootstrap from External byte-wide memory
1	3-4 & 5-6	Bootstrap from SPI
2	1-2 & 5-6	Normal Expanded mode
3	5-6	Development Expanded mode

Table 2-3. Operating Mode Selection

Operating Mode	S4 (ON)	Comment
4	1-2 & 3-4	Host Interface Port Single Strobe mode
5	3-4	Host Interface Port Dual Strobe mode

2.7 Debug LEDs

Six on-board Light-Emitting Diodes, (LEDs), are provided to allow real-time debugging for user programs. These LEDs will allow the programmer to monitor program execution without having to stop the program during debugging; refer to **Figure 2-6**. **Table 2-4**describes the control of each LED.

Table 2-4. LED Control

	Controlled by	
User LED	Port	Signal
LED1	Port D	PD0
LED2	Port D	PD1
LED3	Port D	PD2
LED4	Port D	PD3
LED5	Port D	PD4
LED6	Port D	PD5

Setting PD0, PD1, PD2, PD3, PD4 or PD5 to a Logic One value will turn on the associated LED.

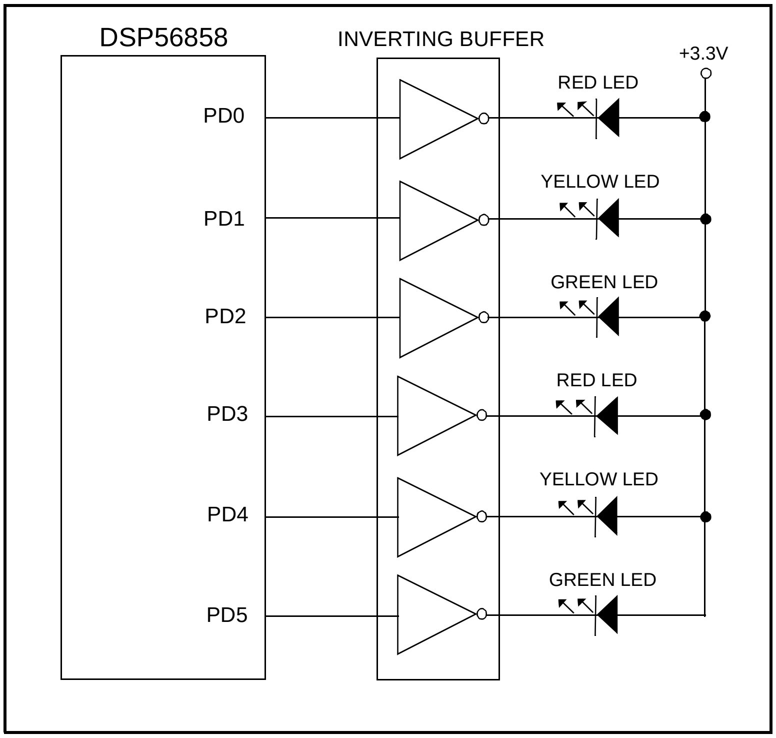


Figure 2-6. Schematic Diagram of the Debug LED Interface

2.8 Debug Support

The DSP56858EVM provides an on-board Parallel JTAG Host Target Interface and a JTAG interface connector for external Target Interface support. Two interface connectors are provided to support each of these debugging approaches. These two connectors are designated the JTAG connector and the Host Parallel Interface Connector.

2.8.1 JTAG Connector

The JTAG connector on the DSP56858EVM allows the connection of an external Host Target Interface for downloading programs and working with the DSP56858's registers. This connector is used to communicate with an external Host Target Interface which passes information and data back and forth with a host processor running a debugger program. **Table 2-5** shows the pin-out for this connector.

Table 2-5. JTAG Connector Description

J3			
Pin #	**Signal**	**Pin #**	**Signal**
1	TDI	2	GND
3	TDO	4	GND
5	TCK	6	GND
7	NC	8	KEY
9	$\overline{\text{RESET}}$	10	TMS
11	+3.3V	12	NC
13	$\overline{\text{DE}}$	14	$\overline{\text{TRST}}$

When this connector is used with an external Host Target Interface, the parallel JTAG interface should be disabled by placing a jumper in jumper block JG5. Reference **Table 2-6** for this jumper's selection options.

Table 2-6. Parallel JTAG Interface Disable Jumper Selection

JG5	Comment
No jumpers	On-board Parallel JTAG Interface Enabled
1–2	Disable on-board Parallel JTAG Interface

2.8.2 Parallel JTAG Interface Connector

The Parallel JTAG Interface Connector, P1, allows the DSP56858 to communicate with a Parallel Printer Port on a Windows PC; reference **Figure 2-7**. Using this connector, the user can download programs and work with the DSP56858's registers. **Table 2-7** shows the pin-out for this connector. When using the parallel JTAG interface, the jumper at JG5 should be removed, as shown in **Table 2-6**.

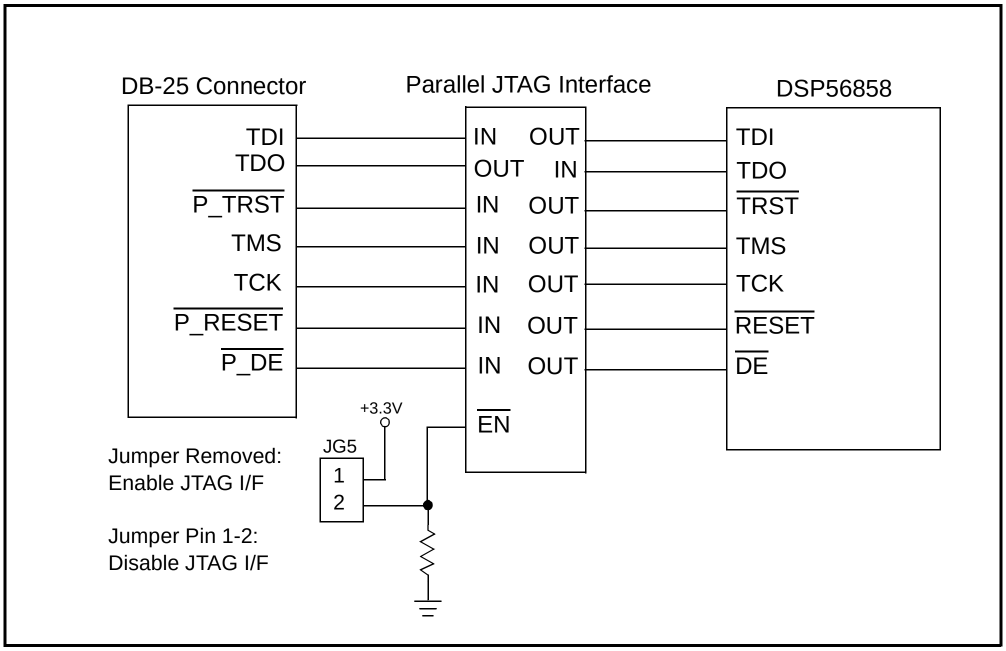


Figure 2-7. Block Diagram of the Parallel JTAG Interface

Table 2-7. Parallel JTAG Interface Connector Description

P1			
Pin #	**Signal**	**Pin #**	**Signal**
1	NC	14	NC
2	PORT_RESET	15	PORT_IDENT
3	PORT_TMS	16	NC
4	PORT_TCK	17	NC
5	PORT_TDI	18	GND
6	PORT_TRST	19	GND
7	PORT_DE	20	GND

Table 2-7. Parallel JTAG Interface Connector Description

P1			
Pin #	**Signal**	**Pin #**	**Signal**
8	PORT_IDENT	21	GND
9	PORT_VCC	22	GND
10	NC	23	GND
11	PORT_TDO	24	GND
12	NC	25	GND
13	PORT_CONNECT		

2.9 External Interrupts

Two on-board push-button switches are provided for external interrupt generation, as shown in **Figure 2-8**. S1 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQA}}$. S2 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQB}}$. These two switches allow the user to generate interrupts for his user-specific programs.

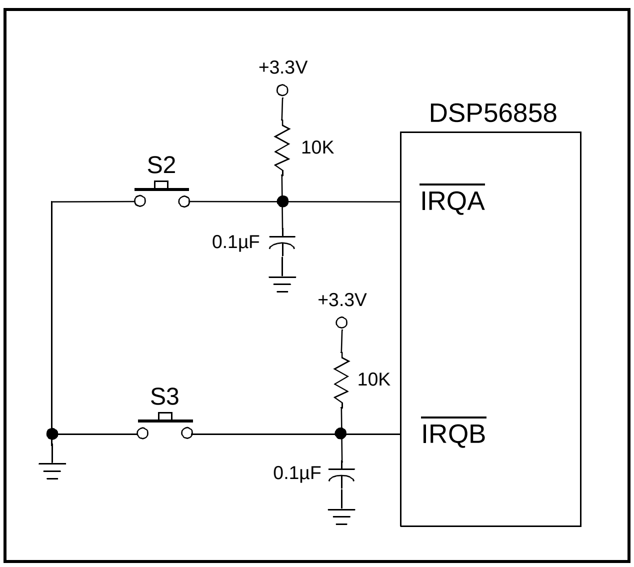


Figure 2-8. Schematic Diagram of the User Interrupt Interface

2.10 Reset

Logic is provided on the DSP56858 to generate an internal Power-On RESET. The DSP56858EVM provides reset logic to support the RESET signals from the JTAG connector, the Parallel JTAG Interface and the user RESET push-button; refer to **Figure 2-9**.

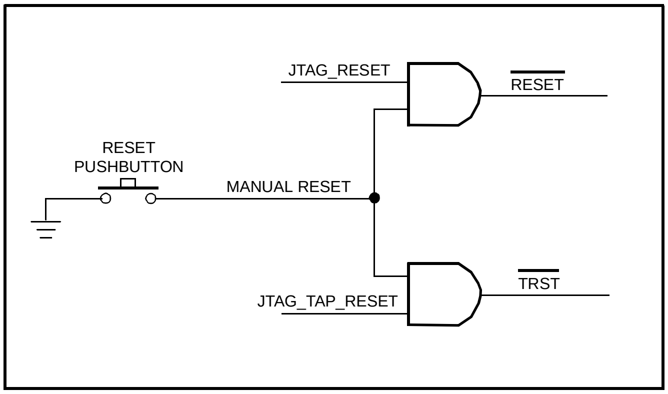


Figure 2-9. Schematic Diagram of the RESET Interface

2.11 Power Supply

The main power input, +12.0V DC/AC, to the DSP56858EVM is through a 2.1mm coax power jack. An optional +5.0V DC power supply input is available through a 2-pin terminal block, TB1. A +12.0V DC 1.2A power supply is provided with the DSP56858EVM; however, less than 500mA is required by the EVM. The remaining current is available for user daughter card applications when connected to the daughter card interface. The power regulation on the DSP56858EVM provides +5.0V DC voltage regulation for the codec's analog circuits and to the additonal voltage regulation logic on the EVM. The additonal voltage regulation logic provides +1.8V DC voltage regulation for the DSP's core and +3.3V DC voltage regulation for the DSP's I/O, memory, parallel JTAG interface and supporting logic; refer to **Figure 2-10**. Power applied to the DSP56858EVM is indicated with a Power-On LED, referenced as LED7.

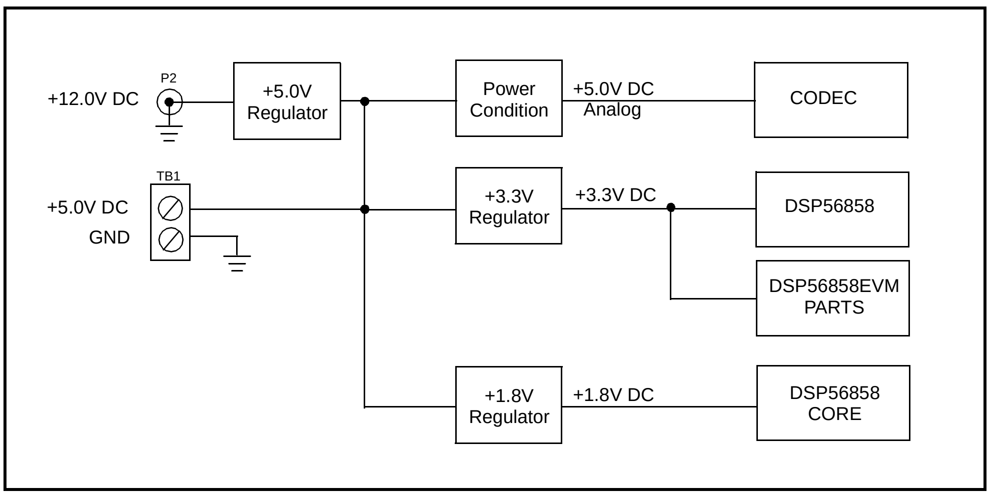


Figure 2-10. Schematic Diagram of the Power Supply

2.12 Stereo Codec

A 16-bit audio-quality stereo codec, Crystal Semiconductor CS4218, is connected to the DSP56858's ESSI port to support audio, voice and signal analysis applications. The codec is clocked with a 12.288MHz oscillator. This allows the codec to operate between a sample frequency of 8KHz and 48KHz. The sample rate can be manually set by setting the appropriate switch positions on DIP switch S5. The sample rate selections possible using this three-position dip switch are detailed in **Table 2-8**. The codec supports +3.3V digital levels, eliminating the need for voltage level translation circuitry. Additionally, a set of zero ohm resistors are provided on the EVM to allow a user to disconnect the on-board codec from the ESSI port and allow him to connect his own codec to the ESSI port; see **Figure 2-12**. The on-board codec has analog signal conditioning logic, allowing direct connection to its line-level input and line-level output signals through two 1/8" stereo jacks; reference **Figure 2-11**.

Table 2-8. Codec Sample Rate Selector

SW 5 Position 3 (MF6)	**SW 5 Position 2** (MF7)	**SW 5 Position 3** (MF8)	**Sample Rate**
ON	ON	ON	48.00KHz
ON	ON	OFF	32.00KHz
ON	OFF	ON	24.00KHz
ON	OFF	OFF	19.20KHz
OFF	ON	ON	16.00KHz
OFF	ON	OFF	12.00KHz
OFF	OFF	ON	9.60KHz
OFF	OFF	OFF	8.00KHz

2.12.1 Analog Input/Output

The DSP56858EVM uses jacks for line-level stereo input, line-level stereo output and stereo headphone output. A National Semiconductor LM4880 provides the drive required for the use of headphones. This device offers a THD, which is superior by a factor of two to the CS4218's on-chip headphone drive circuitry. The basic Analog codec connections are shown in **Figure 2-11**.

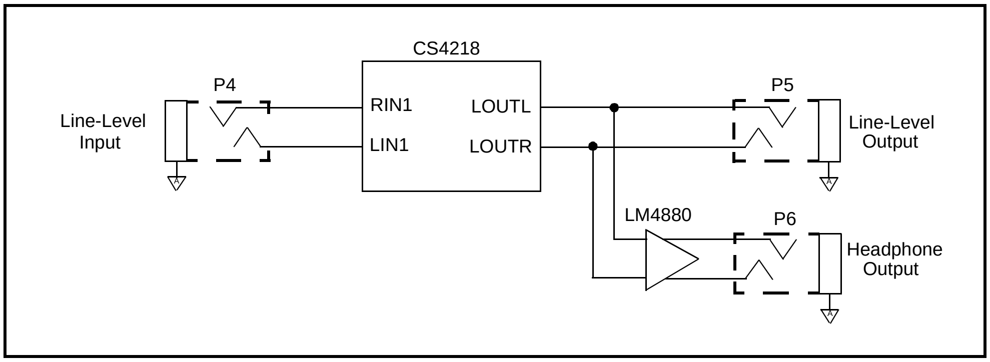


Figure 2-11. CODEC Analog Connections

2.12.2 Digital Interface

The serial interface of the codec transfers digital audio data and control data into and out of the device. The ESSI port consists of independent transmitter and receiver sections and is used for serial communication with the codec.

On the DSP side, the Serial Transmit Data pin, STD0, is an output when data is being transmitted to the codec. The Serial Receive Data pin, SRD0, is an input when data is being received from the codec. These two pins are connected to the codec's Serial Data Input, SDIN, and Serial Data Output, SDOUT, pins.

The DSP's Transmit Serial Clock pin, SCK0, provides the serial bit rate clock for the ESSI interface. It is connected to the CODEC's Serial Port Clock pin, SCLK. Data is transmitted on the rising edge of SCLK and is received on the falling edge of SCLK.

The DSP's GPIO PORT C Bit 4 pin, PC4, is programmed to control the codec's Active Low Reset signal, RESET.

The Serial Transmit Frame Sync pin, SC02, is programmed to control the codec's Frame Sync signal, FSYNC. This signal is sampled by SCLK, with a rising edge indicating a new frame is about to start. The FSYNC frequency is always the system's sample rate. It may be an input to the codec, or it may be an output from the codec in data mode.

The basic codec digital connections are shown in **Figure 2-12**, **Table 2-9** and **Table 2-10**.

The codec's MODE is set by the three MODE selection resistors, R42-R44. In the factory default setting of MODE 4, the codec is set to be the master of the ESSI bus with its data word set at 32 bits per frame; i.e., 16 bits Left channel and 16 bits Right channel. The sample rate is selected on the Sample Rate Selector switch S5; see **Table 2-8** for selection options. Codec control information is sent over a separate serial port using: PC3 as the Control Chip Select signal, CCS; PE2 as the Control Data Input signal, CDIN; and PE3 as the Control Clock signal, CCLK.

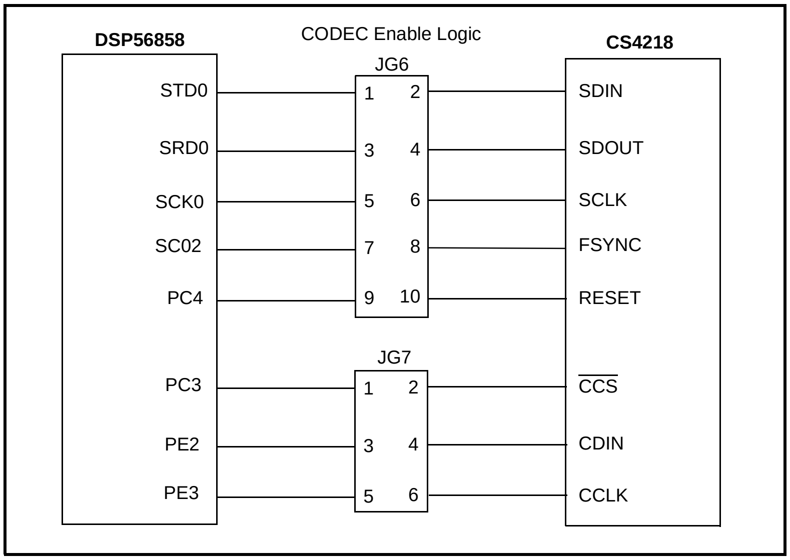


Figure 2-12. CS4218 Stereo Audio Codec

Table 2-9. ESSI Port Connector Description

JG6			
Pin #	**DSP Signal**	**Pin #**	**Codec Signal**
1	STD0	2	SDIN
3	SRD0	4	SDOUT
5	SCK0	6	SCLK
7	SC02	8	FSYNC
9	PC4	10	RESET

Table 2-10. GPIO Port Connector Description

JG7			
Pin #	**DSP Signal**	**Pin #**	**Codec Signal**
1	PC3	2	$\overline{CCS}$
3	PE2	4	CDIN
5	PE3	6	CCLK

2.13 Daughter Card Connectors

The EVM board contains two daughter card expansion connectors. One connector, J1, contains the DSP's external memory bus signals. The other connector, J2, contains the DSP's peripheral port signals.

2.13.1 Memory Daughter Card Expansion Connector

The DSP's external memory bus signals are connected to the Memory Daughter Card Expansion connector, J1. **Table 2-11** shows the port signal-to-pin assignments.

Table 2-11. Memory Daughter Card Connector Description

J1			
Pin #	**Signal**	**Pin #**	**Signal**
1	A10	2	A11
3	A9	4	$\overline{\text{CS1}}$
5	A8	6	A15
7	A7	8	A14
9	A20	10	A19
11	$\overline{\text{WR}}$	12	A13
13	D0	14	A12
15	D1	16	D8
17	D2	18	D9
19	GND	20	GND
21	D3	22	D10
23	D4	24	D11
25	D5	26	D12
27	D6	28	D13
29	A18	30	A17
31	D7	32	D14
33	$\overline{\text{CS0}}$	34	D15
35	A0	36	$\overline{\text{RD}}$
37	A1	38	A6
39	A16	40	GND

J1			
Pin #	**Signal**	**Pin #**	**Signal**
41	A2	42	A5
43	A3	44	A4
45	$\overline{\text{CS3}}$	46	$\overline{\text{CS2}}$
47	+3.3V	48	+3.3V
49	GND	50	GND
51	+5.0V		

2.13.2 Peripheral Daughter Card Expansion Connector

The DSP’s peripheral port signals are connected to the Peripheral Daughter Card Expansion connector, J2. Table 2-12 shows the port signal-to-pin assignments.

Table 2-12. Peripheral Daughter Card Connector Description

J2			
Pin #	**Signal**	**Pin #**	**Signal**
1	$\overline{\text{CS0}}$/PA0	2	$\overline{\text{CS1}}$/PA1
3	CLKO	4	$\overline{\text{CS2}}$/PA2
5	TIO0/PG0	6	TIO1/PG1
7	$\overline{\text{CS3}}$/PA3	8	$\overline{\text{RSTOUT}}$
9	TIO2/PG2	10	TIO3/PG3
11	NC	12	NC
13	GND	14	GND
15	SRD0/PC1	16	SRD1/PD1
17	SC01/PC4	18	SC11/PD4
19	SCK/PF2	20	SCK1/PD2
21	GND	22	GND
23	MOSI/PF1	24	SC10/PD3
25	MISO/PF0	26	SC12/PD5
27	GND	28	GND
29	$\overline{\text{SS}}$/PF3	30	STD1/PD0

Table 2-12. Peripheral Daughter Card Connector Description (Continued)

J2			
Pin #	**Signal**	**Pin #**	**Signal**
31	SC00/PC3	32	MODA/PH0
33	SC02/PC5	34	MODB/PH1
35	$\overline{\text{RESET}}$	36	MODC/PH2
37	GND	38	GND
39	STD0/PC0	40	RXD1/PE2
41	SCK0/PC2	42	TXD1/PE3
43	$\overline{\text{IRQB}}$	44	RXD0/PE0
45	$\overline{\text{IRQA}}$	46	TXD0/PE1
47	+3.3V	48	+3.3V
49	GND	50	GND
51	+5.0V		

2.14 USB

A USB version 2.0 interface controller, NetChip NET2270, is connected to the DSP56858's external address/data bus via CS3. The NET2270 is clocked with a 30.00MHz crystal. This allows the NET2270 interface controller to support the USB Full Speed (12 Mb/sec USB version 1.1) along with the USB High Speed (480 Mb/sec USB version 2.0) bus transfer rates. The NET2270 provides a USB Tranceiver, Serial Interface Engine, USB Protocol Controller, Endpoint FIFOs, Local Bus Interface and Configuration Registers. Refer to the USB diagram in **Figure 2-13**. The USB Interface's use of CS3 can be disabled by removing the jumper at JG11.

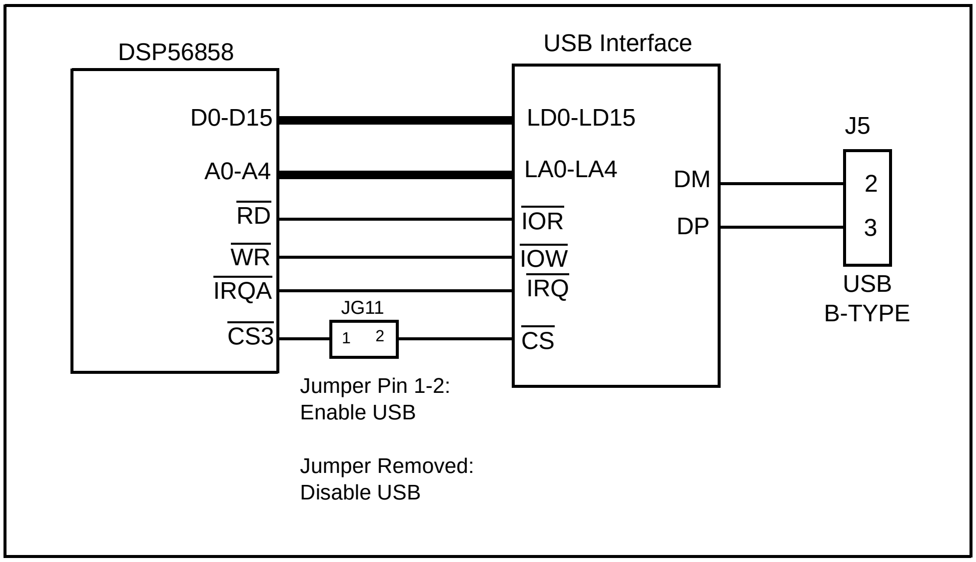


Figure 2-13. Diagram of the USB Interface

2.15 Host Interface Connector

The DSP56858EVM board contains a Host Interface connector. The HI connector, J4, provides the signals present on the DSP56858's HI port. **Table 2-13** shows the HI connectors signal-to-pin assignments.

Table 2-13. Host Interface Connector Description

J4			
Pin #	**Signal**	**Pin #**	**Signal**
1	HD0	2	HD1
3	HD2	4	HD3
5	HD4	6	HD5
7	HD6	8	HD7
9	HA0	10	HA1
11	HA2	12	HRW
13	$\overline{HDS}$	14	$\overline{HCS}$
15	$\overline{HREQ}$	16	$\overline{HACK}$
17	+3.3V	18	GND
19	+3.3V	20	GND

2.16 Test Points

The DSP56858EVM board has a total of seven test points. Three digital GND test points are located in corners of the board. The +5.0VA and AGND test points are located in the analog corner of the board. The +1.8V and +3.3V test points are located in the power supply section of the board.

Appendix A
DSP56858EVM Schematics

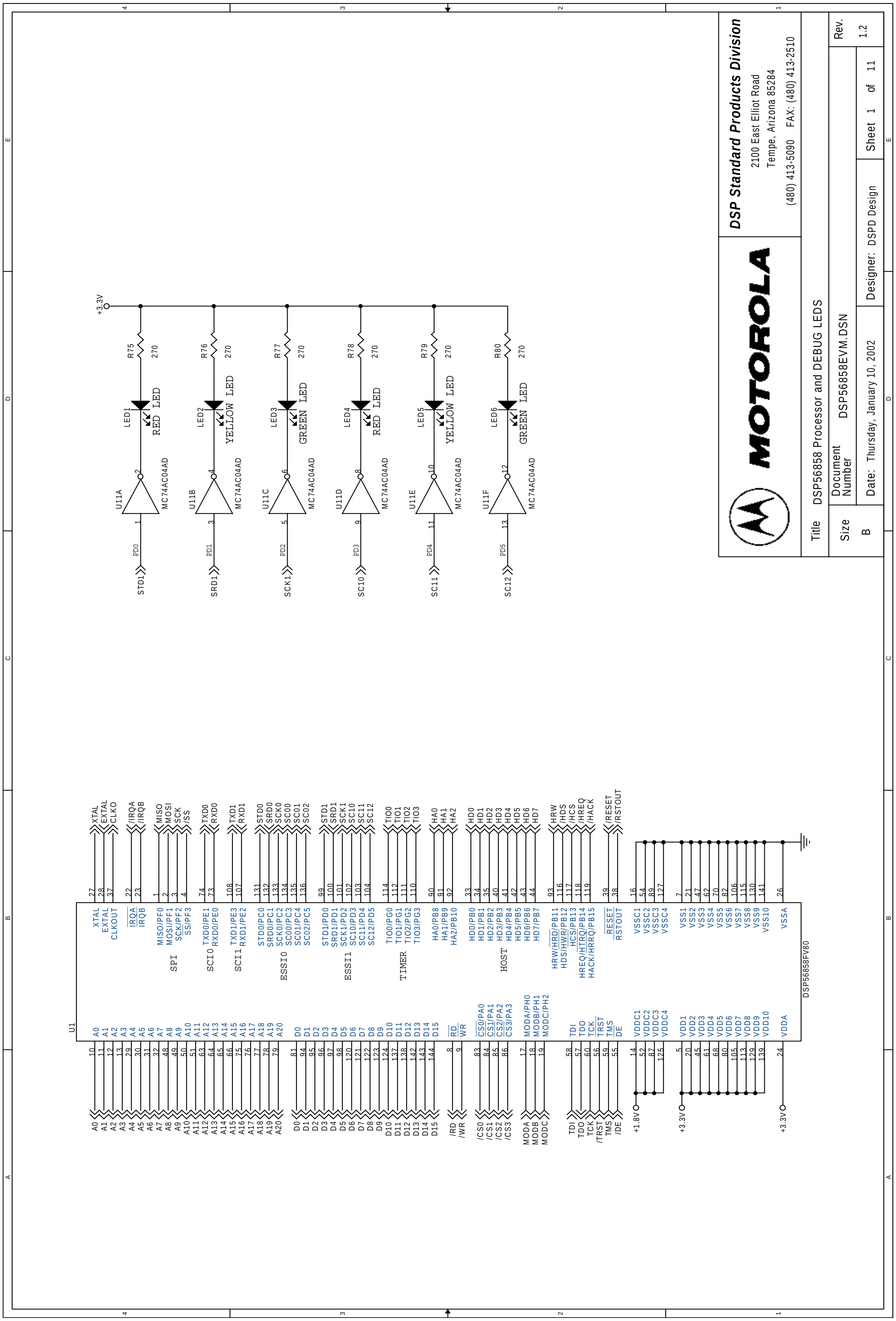


Figure A-1. DSP56858 Processor and DEBUG LEDS

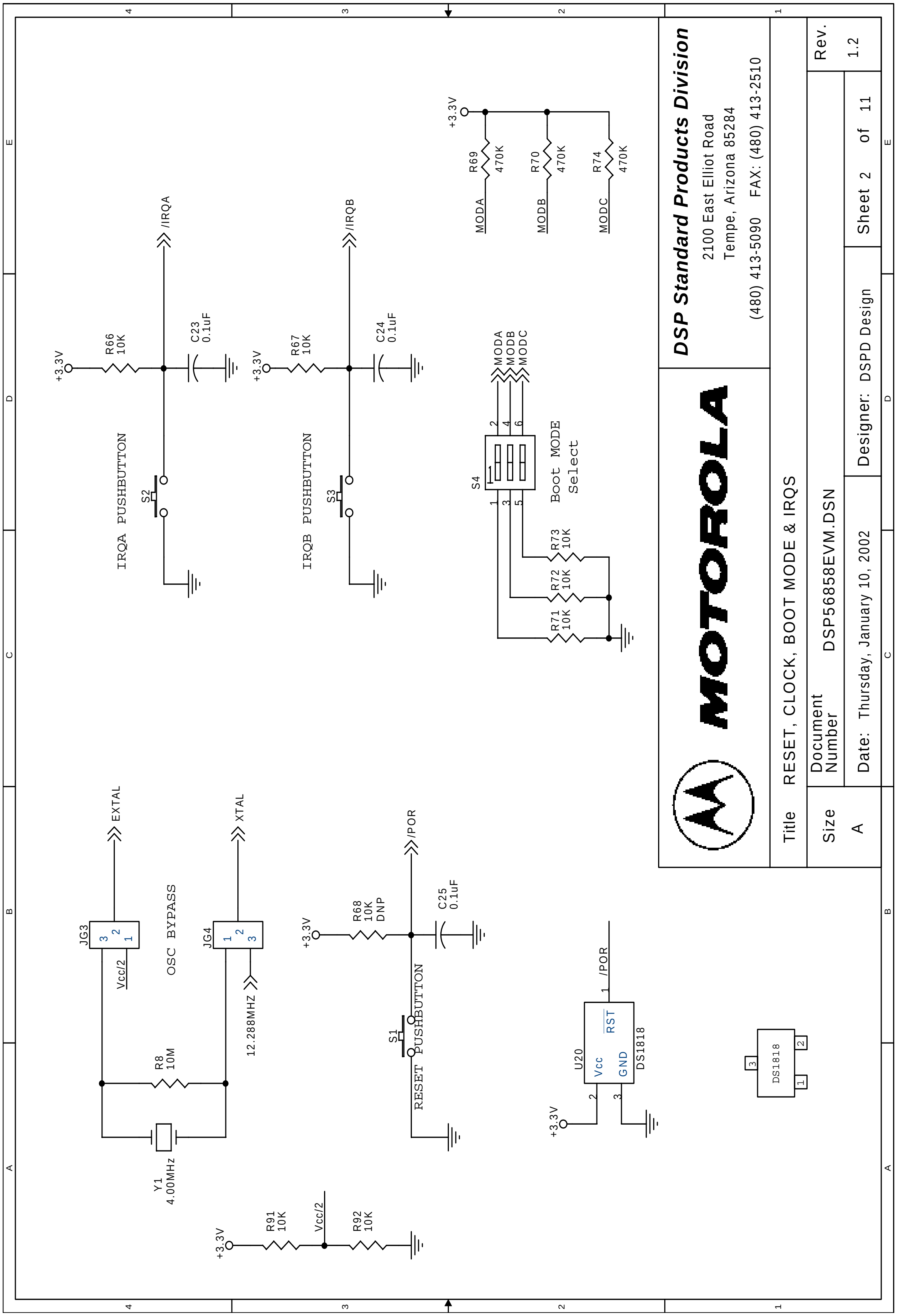


Figure A-2. RESET, CLOCK, BOOT MODE & IRQs

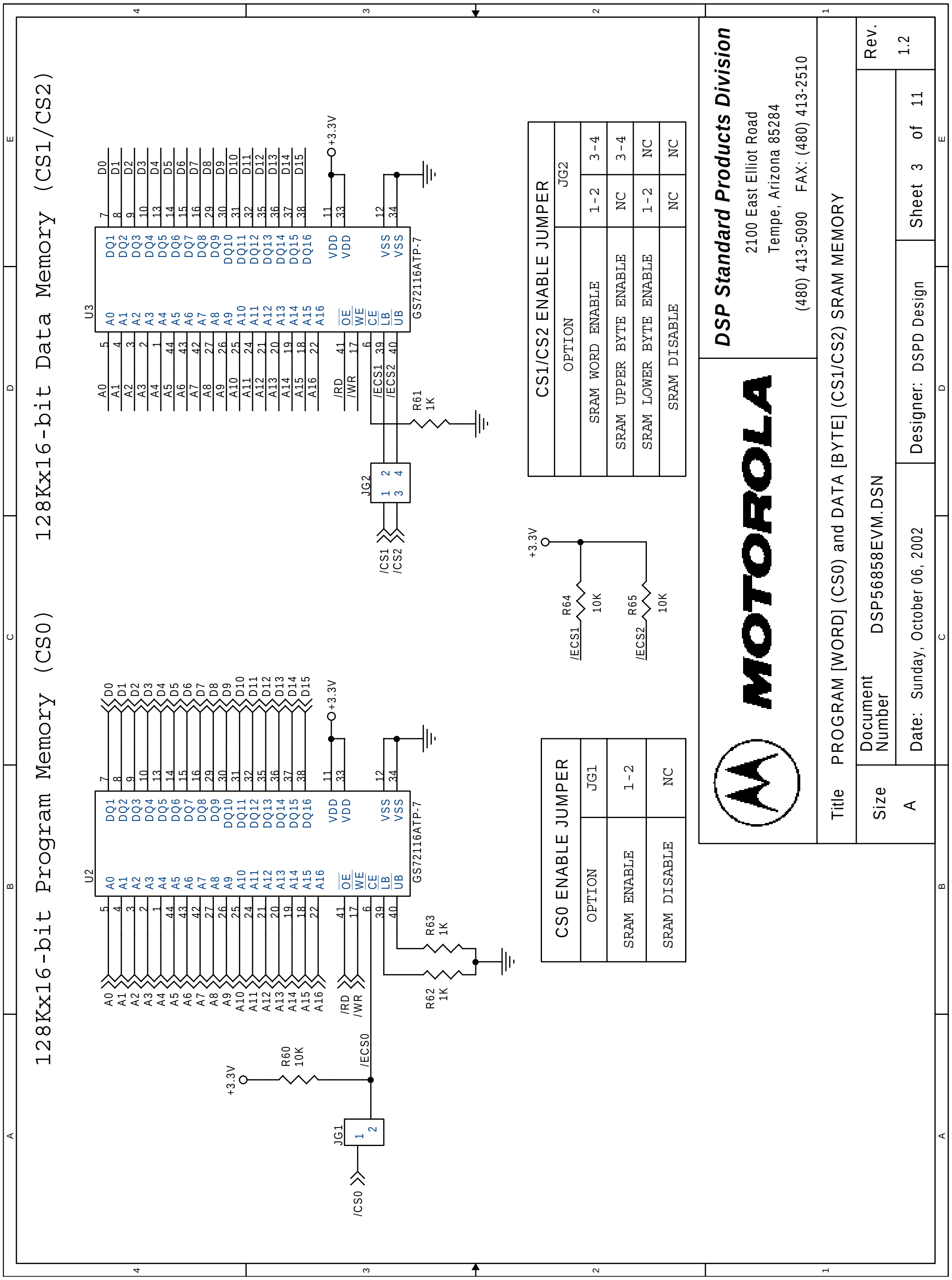


Figure A-3. Program [Word] (CS0) & Data [Byte] (CS1/CS2) SRAM Memory

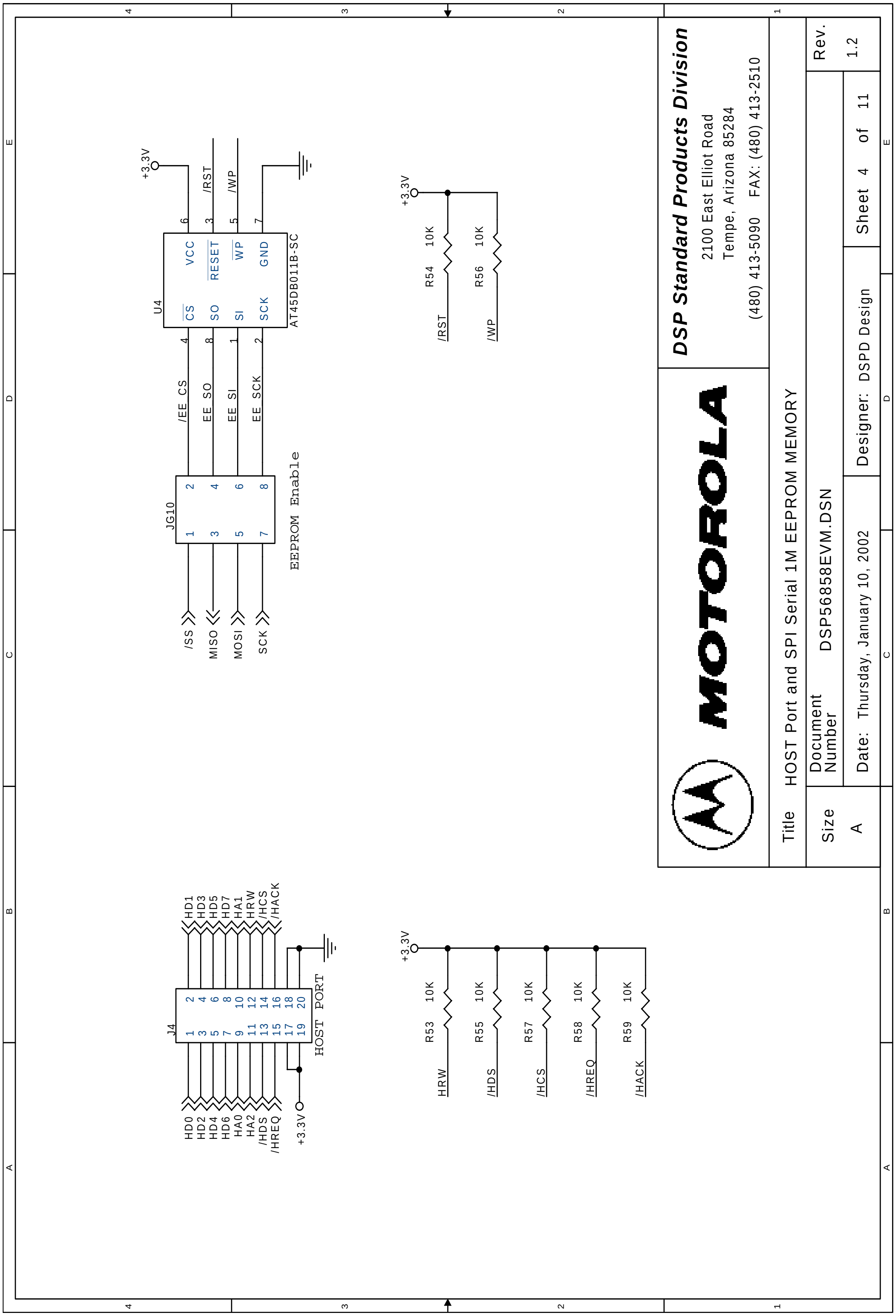


Figure A-4. HOST Port and SPI Serial 1M-bit Serial EEPROM Memory

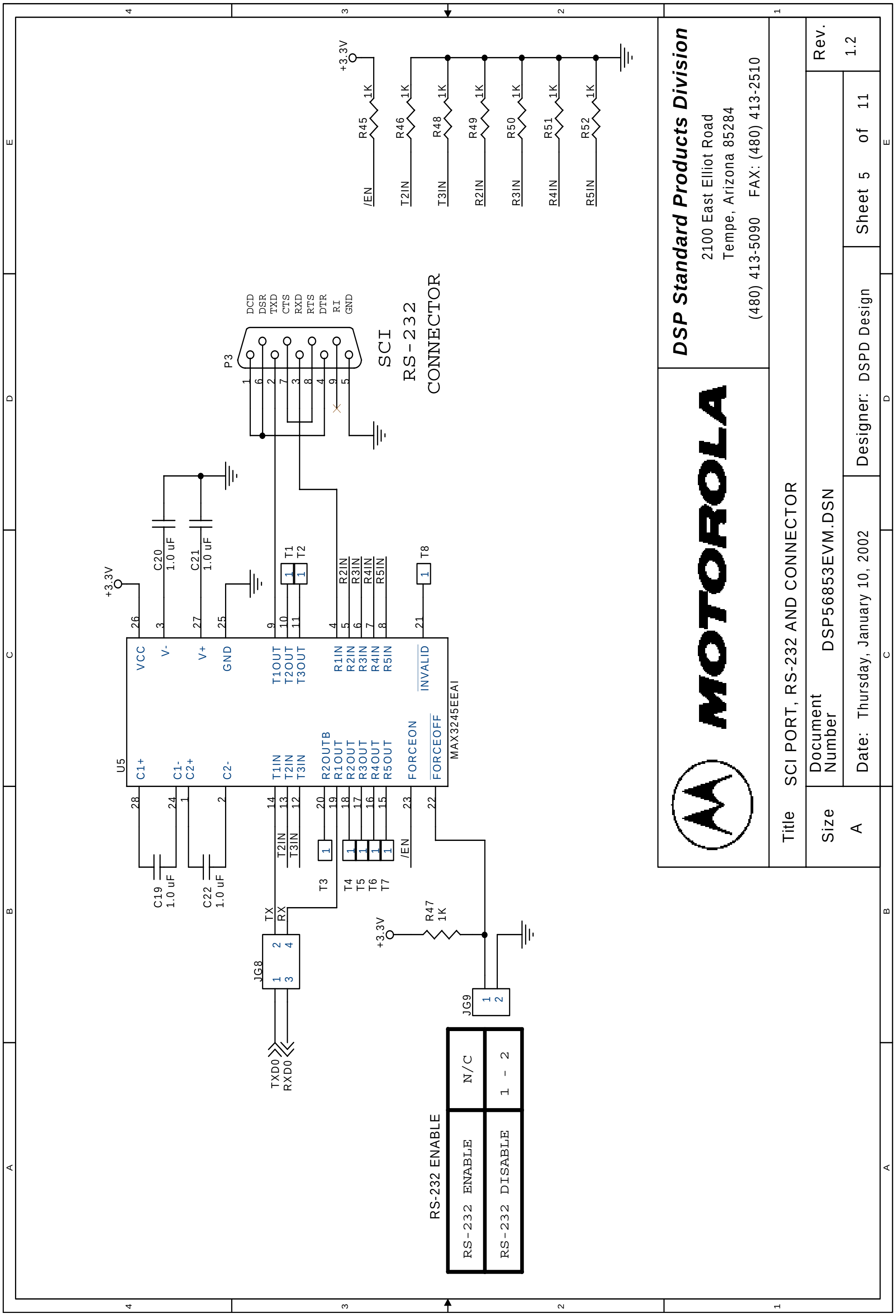


Figure A-5. SCI PORT, RS-232 and Connector

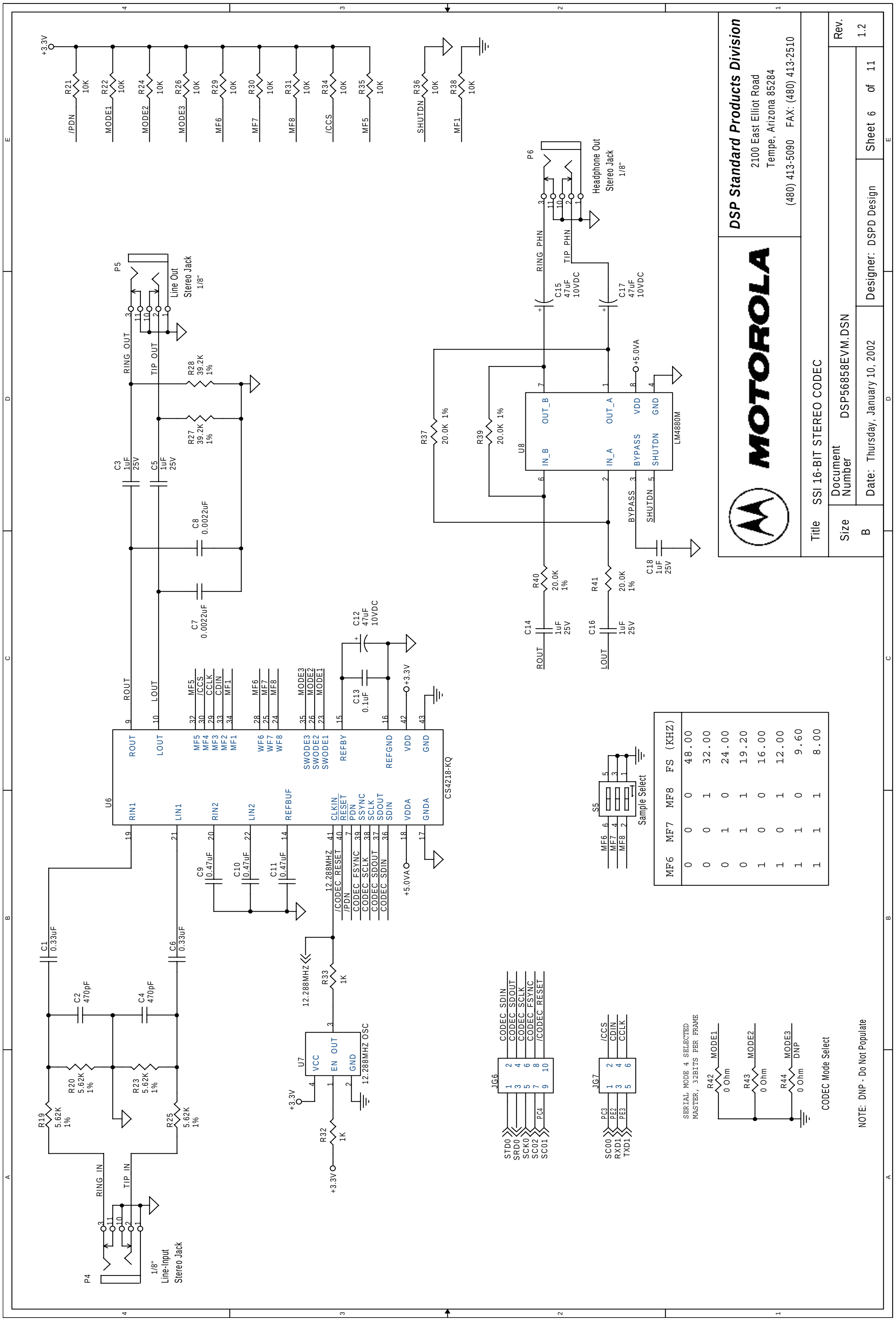


Figure A-6. SSI 16-Bit Stereo Codec

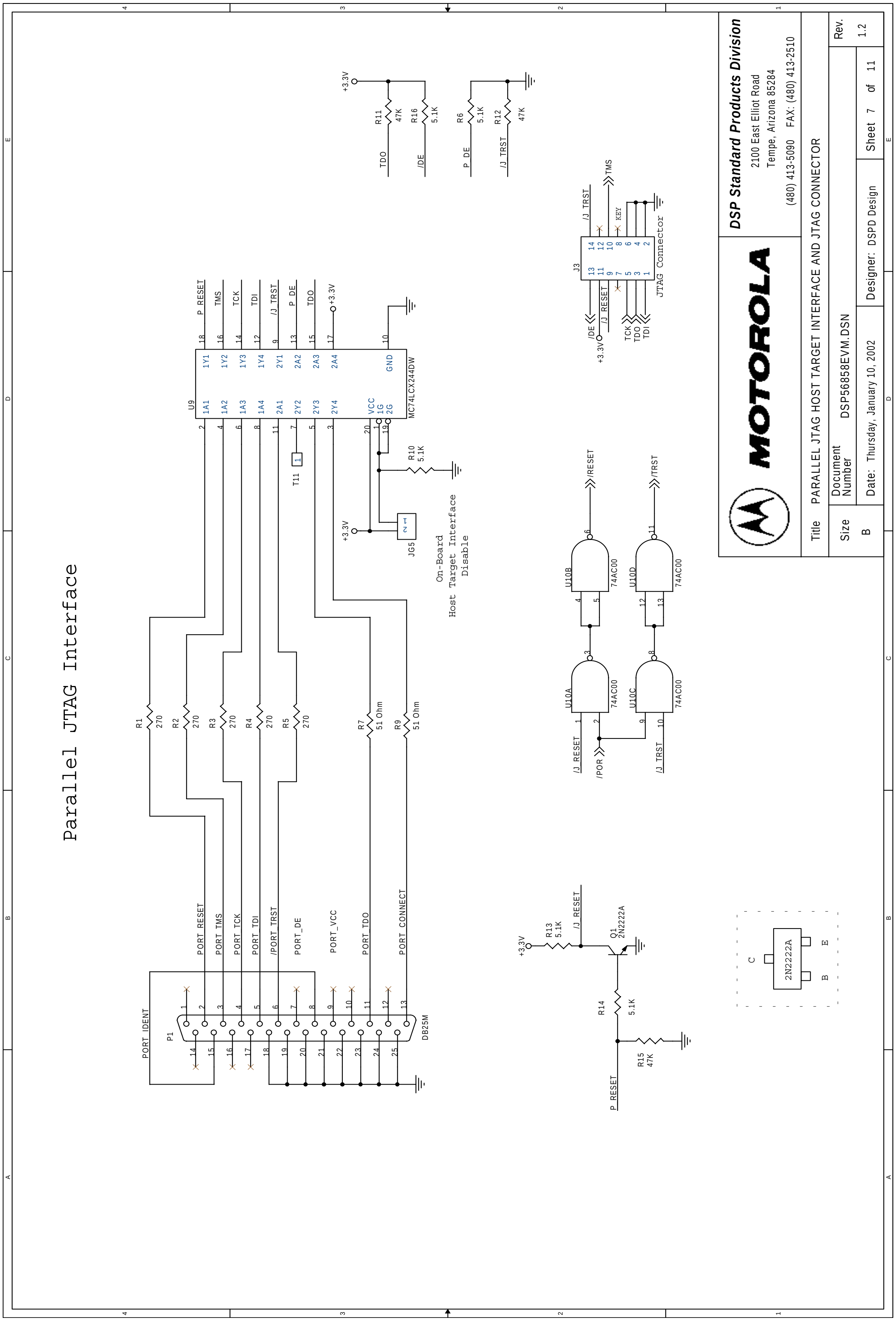


Figure A-7. Parallel JTAG Host Target Interface and JTAG Connector

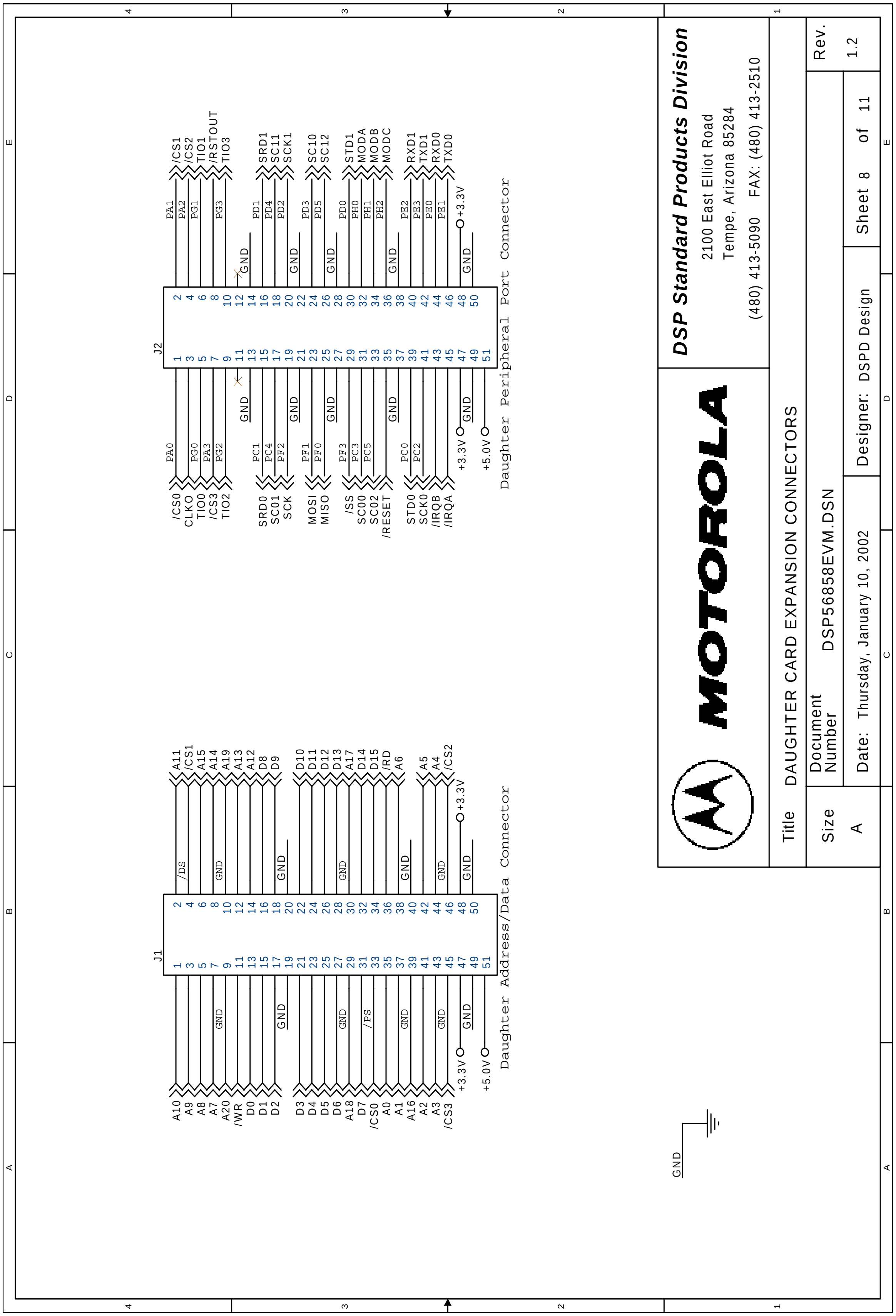


Figure A-8. Daughter Card Expansion Connectors

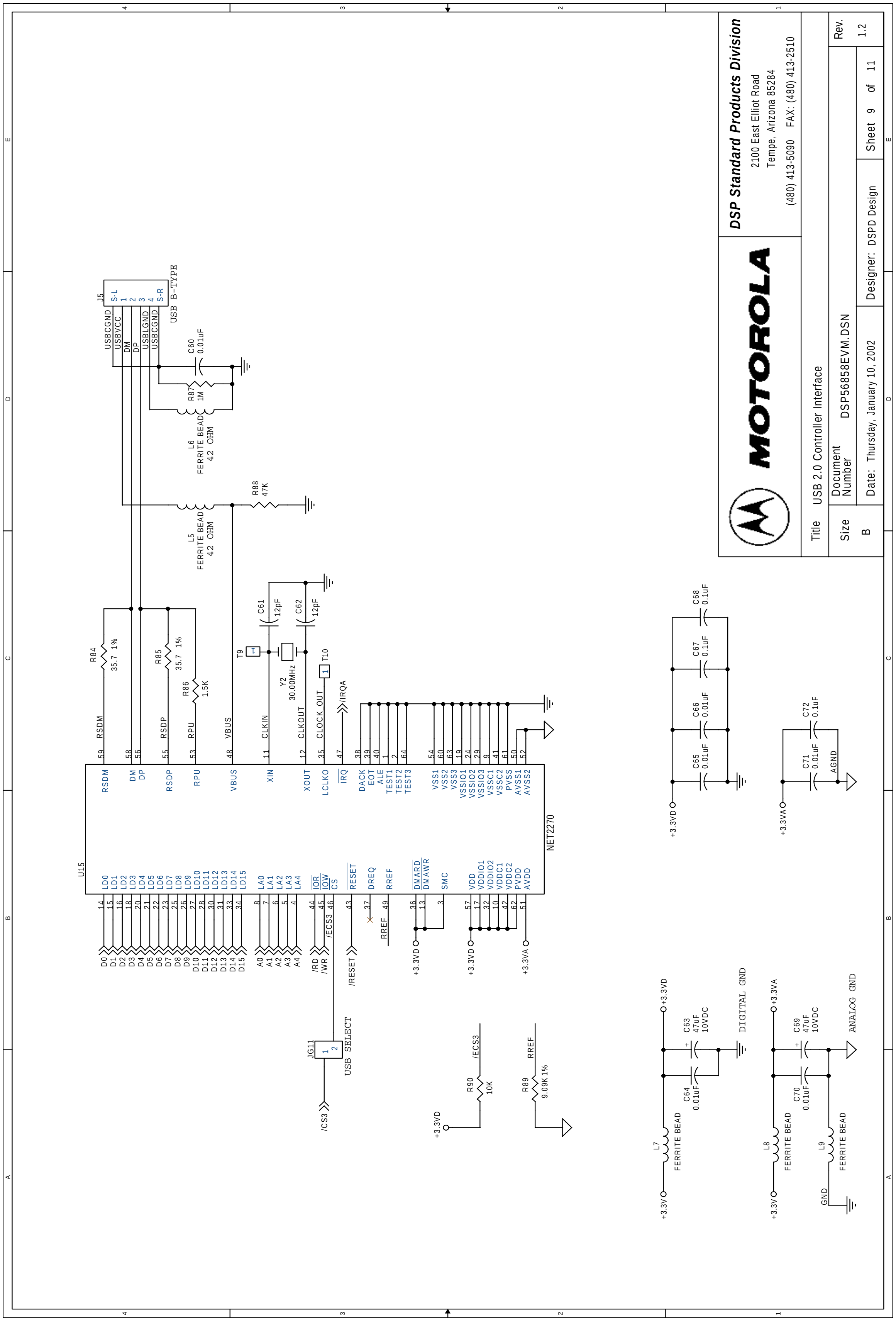


Figure A-9. USB 2.0 Controller Interface

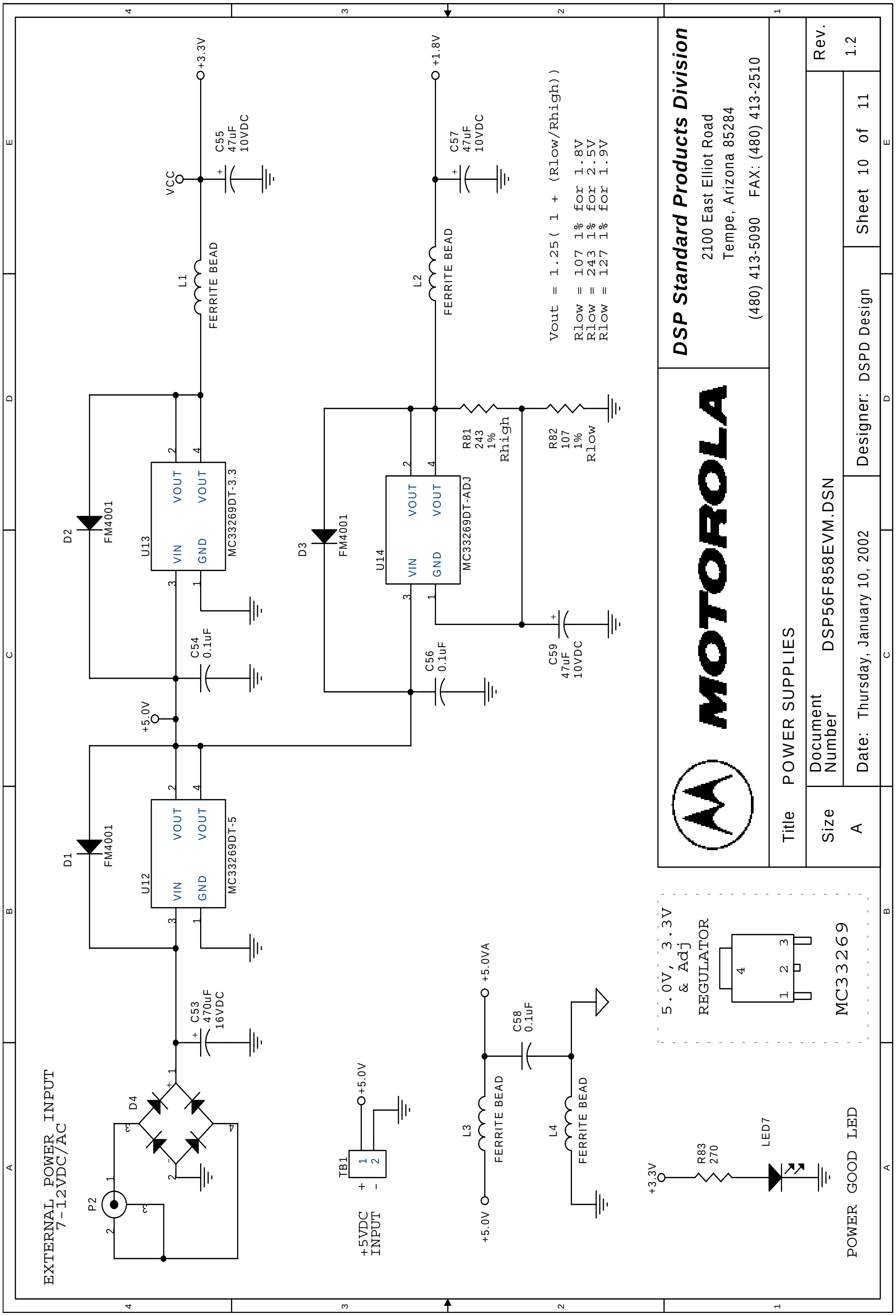


Figure A-10. POWER SUPPLIES

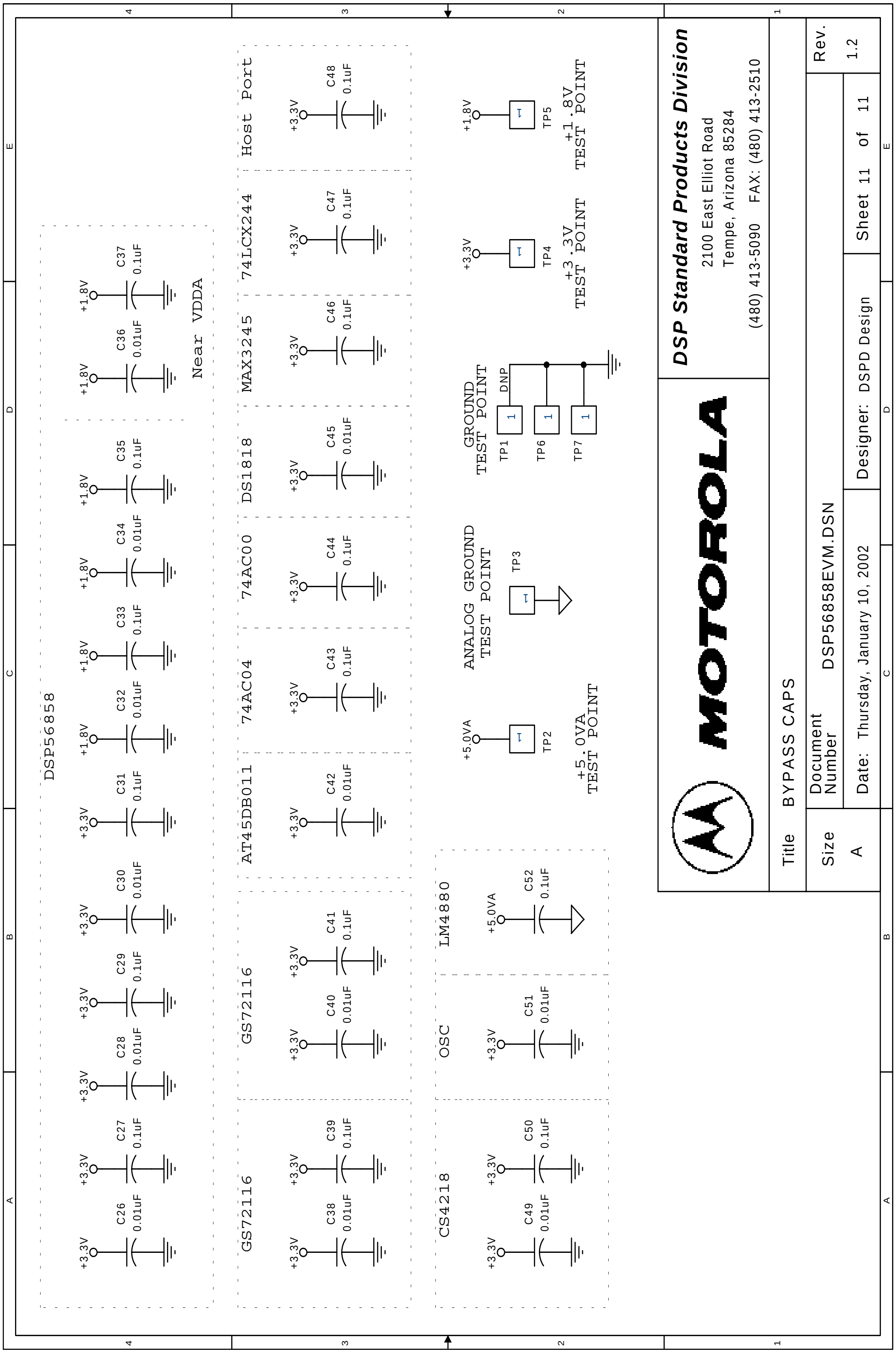


Figure A-11. POWER SUPPLIES

Appendix B
DSP56858EVM Bill of Material

Qty	Description	Ref. Designators	Vendor Part #
Integrated Circuits			
1	DSP56858	U1	Motorola, DSP56858FV120
2	GS72116	U2, U3	GSI, GS72116ATP-7
1	AT45DB011	U4	Atmel, AT45DB011B-SC
1	MAX3245	U5	Maxim, MAX3245EEAI
1	CS4218	U6	Crystal Semiconductor, CS4218-KQ
1	12.288MHz OSC	U7	Epson, SG-531P-12.288MC
1	LM4880	U8	National Semiconductor, LM4880M
1	74LCX244	U9	ON Semiconductor, MC74LCX244ADW
1	74AC00	U10	Fairchild, 74AC00SC
1	74AC04	U11	ON Semiconductor, MC74AC04AD
1	+5.0V Voltage Regulator	U12	ON Semiconductor, MC33269DT-5
1	+3.3V Voltage Regulator	U13	ON Semiconductor, MC33269DT-3.3
1	+1.8V Voltage Regulator	U14	ON Semiconductor, MC33269DT-ADJ
1	NET2270	U15	NetChip, NET2270
1	DS1818	U20	Dallas Semiconductor, DS1818
Resistors			
12	270 Ω	R1 - R5, R75 - R80, R83	SMEC, RC73L2A270OHMJT
5	5.1K Ω	R6, R10, R13, R14, R16	SMEC, RC73L2A5.1KOHMJT
2	51 Ω	R7, R9	SMEC, RC73L2A51OHMJT
1	10M Ω	R8	SMEC, RC73L2A10MOHMJT
4	47K Ω	R11, R12, R15, R88	SMEC, RC73L2A47KOHMJT

Qty	Description	Ref. Designators	Vendor Part #
4	5.62K Ω, 1%	R19, R20, R23, R25	SMEC, RC73L2A5.62KOHMFT
29	10K Ω	R21, R22, R24, R26, R29-R31, R34-R36, R38, R53-R60, R64-R67, R71-R73, R90-R92	SMEC, RC73L2A10KOHMJT
2	39.2K Ω, 1%	R27, R28	SMEC, RC73L2A39.2KOHMFT
13	1K Ω	R32, R33, R45-R52, R61-R63	SMEC, RC73L2A1KOHMJT
4	20.0K Ω, 1%	R37, R39-R41	SMEC, RC73L2A20.0KOHMFT
2	0 Ω	R42, R43	SMEC, RC73JP2A
0	0 Ω	R44	SMEC, RC73JP2A
0	10K Ω	R68	SMEC, RC73L2A10KOHMJT
3	470K Ω	R69, R70, R74	SMEC, RC73L2A470KOHMJT
1	243 Ω, 1%	R81	SMEC, RC73L2A243OHMFT
1	107 Ω, 1%	R82	SMEC, RC73L2A107OHMFT
2	35.7 Ω, 1%	R84, R85	SMEC, RC73L2A35.7OHMFT
1	1.5K Ω	R86	SMEC, RC73L2A1.5KOHMJT
1	1M Ω	R87	SMEC, RC73L2A1MOHMJT
1	9.09K Ω, 1%	R89	SMEC, RC73L2A9.09KOHMFT
Inductors			
4	1.0mH FERRITE BEAD	L1 - L4	Panasonic, EXC-ELSA35V
5	FERRITE BEAD	L5 - L9	TOKO, FLSM2520-1R0J
LEDs			
2	Red LED	LED1, LED4	Hewlett-Packard, HSMS-C650
2	Yellow LED	LED2, LED5	Hewlett-Packard, HSMY-C650
3	Green LED	LED3, LED6, LED7	Hewlett-Packard, HSMG-C650
Diode			
1	S2B-FM401	D1	Vishay, DL4001DICT
1	+50V 1A BRIDGE RECT	D2	DIODES, DF02S

Qty	Description	Ref. Designators	Vendor Part #
		Capacitors	
2	0.33µF	C1, C6	SMEC, MCCE334K3NR-T1
2	470pF	C2, C4	SMEC, MCCE471J2NO-T1
9	1.0µF, +25V DC	C3, C5, C14, C16, C18-C22	SMEC, MCCE105K3NR-T1
2	0.0022µF	C7, C8	SMEC, MCCE222K2NR-T1
3	0.47µF	C9-C11	SMEC, MCCE474K3NR-T1
8	47µF, +16V DC	C12, C15, C17, C55, C57, C59, C63, C69	ELMA, RV2-16V470M-R
25	0.1µF	C13, C23-C25, C27, C29, C31, C33, C35, C37, C39, C41, C43, C44, C46-C48, C50, C52, C54, C56, C58, C67, C68, C72	SMEC, MCCE104K2NR-T1
18	0.01µF	C26, C28, C30, C32, C34, C36, C38, C40, C42, C45, C49, C51, C60, C64-C66, C70, C71	SMEC, MCCE103K2NR-T1
1	470µF, +16V DC	C53	ELMA, RV-16V471MH10R
2	15pF	C61, C62	SMEC, MCCE150J2NO-T1

		Jumpers	
4	1 × 2, 2mm Header	JG1, JG5, JG9, JG11	SAMTEC, TMM-102-02-S-S
2	2 x 2, 2mm Header	JG2, JG8	SAMTEC, TMM-102-02-S-D
2	3 × 1, 2mm Header	JG3, JG4	SAMTEC, TMM-103-02-S-S
1	5 x 2, 2mm Header	JG6	SAMTEC, TMM-105-02-S-D
1	3 x 2, 2mm Header	JG7	SAMTEC, TMM-103-02-S-D
1	4 × 2, 2mm Header	JG10	SAMTEC, TMM-104-02-S-D
		Test Points	
4	Black Test Point	TP1, TP3, TP6, TP7	Keystone, 5001
1	Red Test Point	TP2	Keystone, 5000
1	White Test Point	TP4	Keystone, 5002
1	Yellow Test Point	TP5	Keystone, 5004

Crystals			
1	4.00MHz Crystal	Y1	CTS, ATS04ASM-T
1	30.00MHz Crystal	Y2	Epson, MA-306 30.000M-C2
Connectors			
1	DB25M Connector	P1	AMPHENOL, 617-C025P-AJ121
1	2.1mm coax Power Connector	P2	Switchcraft, RAPC-722
1	DE9S Connector	P3	AMPHENOL, 617-C009S-AJ120
3	1/8” Stereo Jack	P4 - P6	Switchcraft, 35RAPC4BHN2
2	51-Pin HD Connector	J1, J2	BERG, 91930-21151
1	7 x 2 Bergstick	J3	SAMTEC, TSW-107-07-S-D
1	10 x 2 RT Bergstick	J4	SAMTEC, TSW-110-07-S-D-RT
1	Type B USB	J5	Mill-Max, 897-30-004-90-000000
1	2-Pin Terminal Block	TB1	On-Shore Technology, ED500/2DS
Switches			
3	SPST Pushbutton	S1 - S3	Panasonic, EVQ-PAD05R
2	3-Position DIP SW	S4, S5	CTS, 209-3LPST
Transistors			
1	2N2222A	Q1	ZETEX, FMMT2222ACT
Miscellaneous			
20	2mm Shunt	SH1 - SH20	Samtec, 2SN-BK-G
4	Rubber Feet	RF1 - RF4	3M, SJ5018BLKC

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